

SiS Flexible Design Solutions

SiSM661MX/648MX/963




Pentium M Architecture Chipset

**Silicon Integrated Systems Corp.
Integrated Product Division
Dec, 2003**



Agenda

- ❖ SiS roadmap update
- ❖ Chipset introduction

	Mass Production	Q1'04	Q2'04	Q3'04
Performance	 <p>648MX, Pentium M DDR400, AGP8X MP: Now</p>			
Mainstream	 <p>M661MX, Pentium M DDR400, AGP8X Real256E GPU MP: Now</p>			
Value	 <p>M652, Pentium M DDR333, AGP4X Real256 GPU MP: Now</p>			

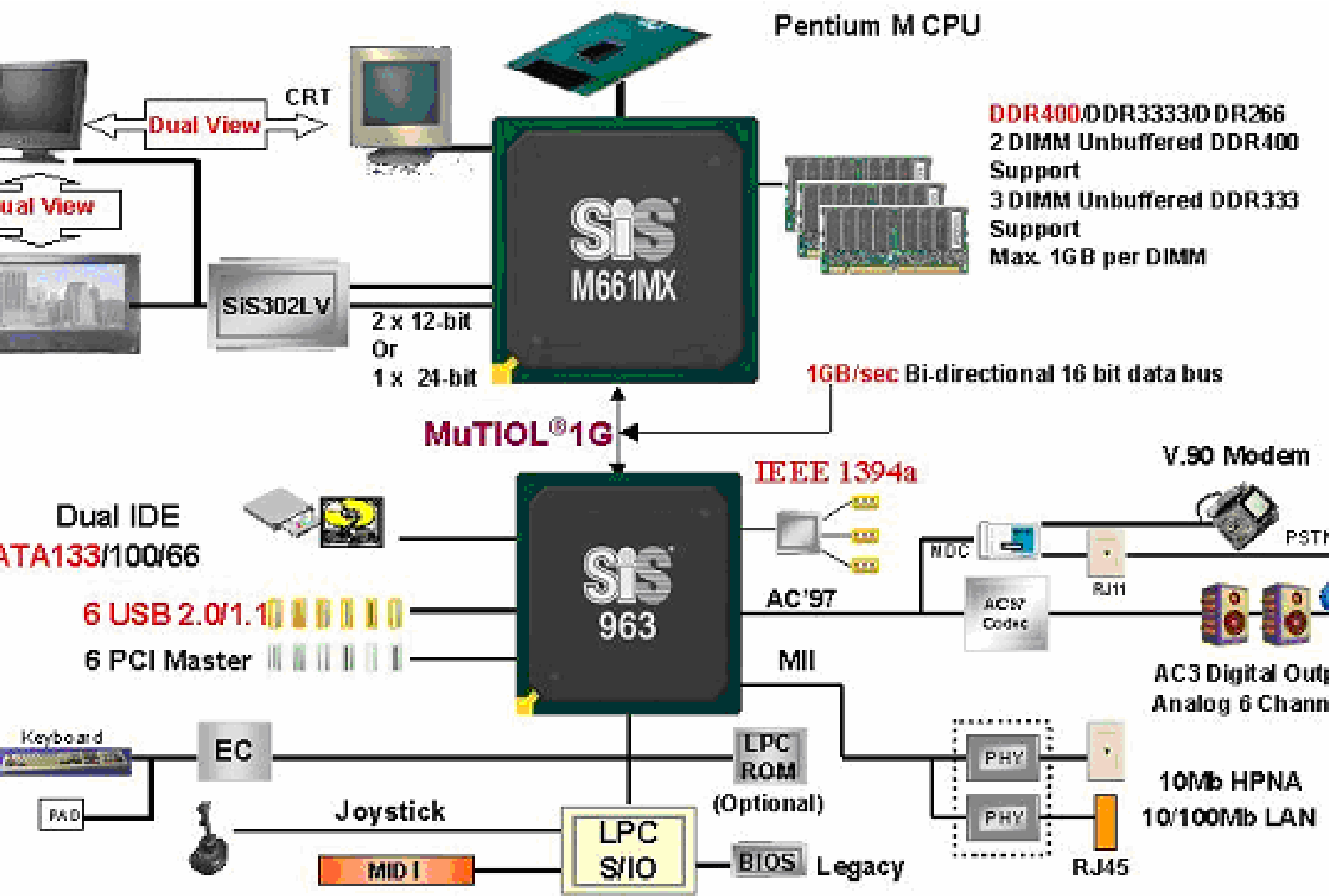
Chipset Introduction

- ❖ SiS Integrated Product History
- ❖ SiSM661MX/SiS648MX Family w/ SiS963 Block Diagram
- ❖ Feature List
- ❖ Performance Analysis
- ❖ S/W Information
- ❖ SiS Technology
- ❖ Schedule Information
- ❖ Third Party Information



	1998		1999		2000		2001		2003	
	1H	2H	1H	2H	1H	2H	1H	2H	1H	
Graphic Products Roadmap	<p>SiS 6326</p> <ul style="list-style-type: none"> • 64-bit 2D/3D Engine • 64-bit Memory Bus <p>SiS 300</p> <ul style="list-style-type: none"> • 128-bit 2D/3D Engine • 128/64-bit Memory Bus • MCLK:133MHz <p>MP:Now</p> <p>SiS 305</p> <ul style="list-style-type: none"> • 128-bit 2D/3D Engine • 64-bit Memory Bus • MCLK:125MHz <p>MP:Now</p> <p>SiS 315</p> <ul style="list-style-type: none"> • 256 bit New3D Engine • 128/64 bit Memory Bus • 2'nd Gen. T&L engine • Hyper FSAA • Dx8 Compatible • MCLK:166Mhz <p>MP:Now</p> <p>SiS 530 620</p> <p>SiS 630S 730S</p> <p>3DMark 2001 > 900 3D WB > 25 FPS</p> <p>SiS 650/651 740 M652</p> <p>3DMark 2001 > 1300 3D WB > 37 FPS</p> <p>SiS 661 M661 M662</p> <p>3DMark 2001 > 2200 3D WB</p>									
Integration sets	<p>Diagram showing integration sets and performance benchmarks for various SiS products, including 3DMark 2001 scores and 3D WB FPS.</p>									

SIS M661MX/963 System Architecture



Host Interface

- Support Intel Pentium M Hyper Threading CPU
- FSB **533/400MHZ** w/ 2X Address and 4X Data Rate
- 12 Outstanding Transactions support
- Quasi-Synchronous/Asynchronous Host/DRAM Timing support
- Support 2M/4M/8M/16M TSEG SMRAM
- Support Dynamic Bus Inversion.

DRAM Controller

- **DDR400**/DDR333/DDR266 Support
- Support Up to 2 un-buffered DIMMs DDR400
- Support Up to 3 un-buffered DIMMs DDR333/266
- Up to 1GB per DIMM with 512Mb tech.
- Dynamic Clock Enable (CKE) control placing the Memory into Suspend to DRAM state.

AGP3.5 and **AGP2.0** Compliant

- 8X/4X Mode Support
- Fast Write Support
- Support 1.5V interface only

SiS MuTIOL Technology Delivering **1GB/sec Bandwidth**

DX9 S/W Compliant

High performance 256Bit 3D/128Bit 2D Graphic Engine

- 2 pixel rendering pipelines and 4 texture units per cycle (2P4T)
- Up to **200 MHz** ECLK

SiS Ultra-AGP II™ Technology w/ up to 3.2GB/s Data Transfer Rate

- Successor of Ultra-AGP II™ Technology and double the bandwidth up to 3.2GB/s w DDR400
- AGP8X equivalent bandwidth for 3D/2D/Video

Advanced Hardware Acceleration for DVD playback

Share Memory Size 32MB and 64MB

Dual 12-bit DDR Digital Interface for Digital LCD/TV-OUT support

- NTSC/PAL TV-OUT
- DVI LCD Monitor
- Dual view function support for LCD-TV, LCD-CRT or CRT-TV

Built-in high performance 333MHz RAMDAC

Graphic support mode

- CRT highest resolution mode: 2048x1536x32@75NI
- LCD highest resolution mode: 1600x1200x32@ 60NI

USB 2.0/1.1 Support

- Integrated Two Independent Open HCI Controllers includes Root Hub w/ two USB 1.1 ports each
- Integrated One EHCI Controller includes Root Hub w/ six USB 2.0 ports
- Support a maximum of 6 USB Ports. Dynamic connection to USB 1.1 or USB 2.0.

IDE Controller

- Dual Independent IDE Channels with **ATA133**/100/66 support

Integrated MAC Controller with Standard MII Interface

Integrated Audio Controller w/ AC97 2.2 Compliance Interface

- Support **5.1 channel of Audio output** and V.90 HSP Modem
- Support 4 Separate SDATAIN Pins for 3 x 2 ch Audio Codec + 1 Modem Codec

3 ports IEEE 1394a

PCI 2.2 Compliant

- Support up to 6 PCI Masters

LPC Interface 1.0 Compliance

ACPI 1.0b Compliance

I/O APIC Support

PC2001 Compliance

SiS MuTIOL Technology Delivering 1GB/sec Bandwidth

Support Intel CPU Speed Step Technology

Advanced Power Management ACPI 1.0b Compliance

Sleeping States

- S0: Normal Run
- S1: Internal CPU Clock Stop
- S3: Suspend-To-DRAM
- S4 : Suspend-To-HDD
- S5: System Power Off

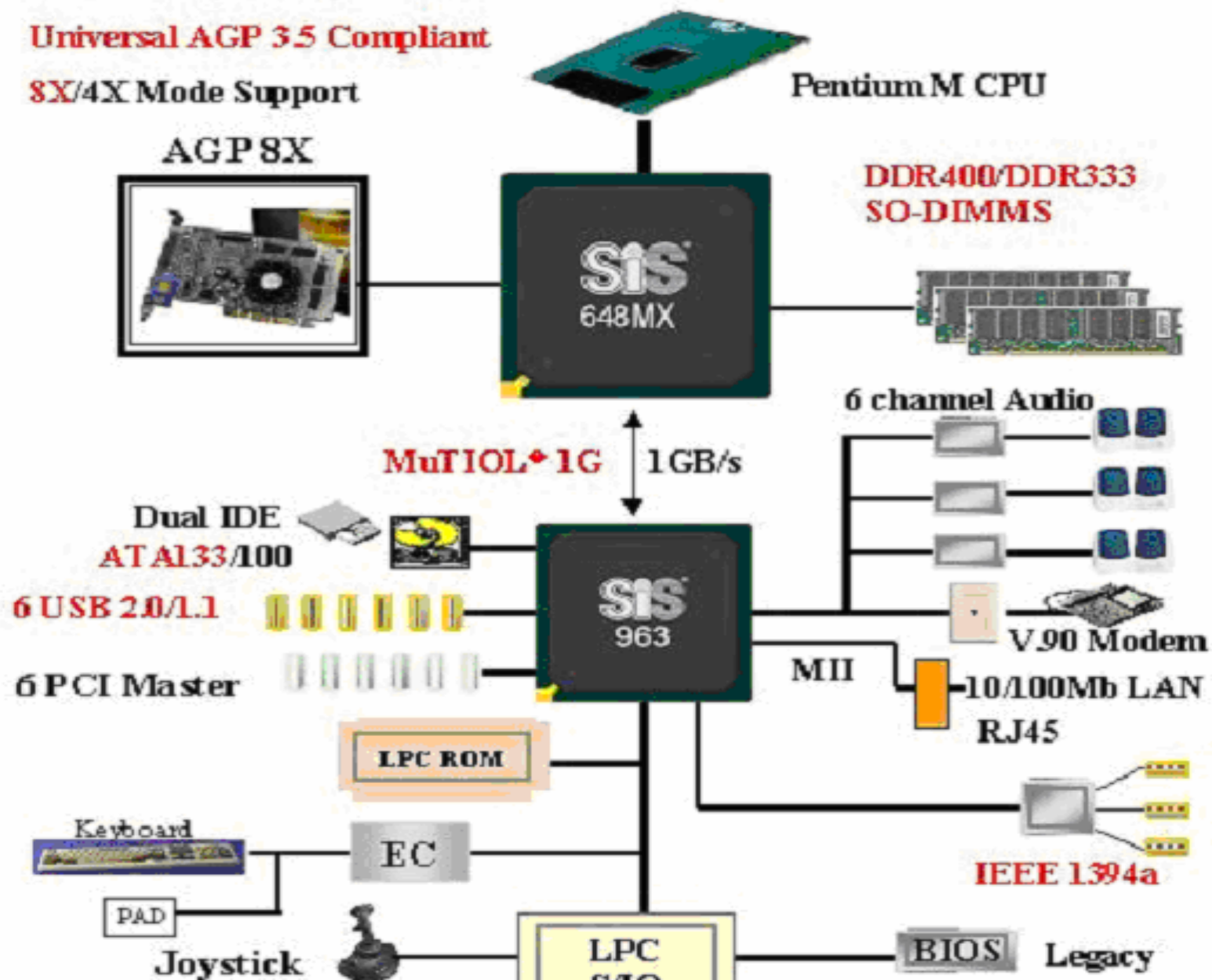
Processor Power States

- C0, C1, C2, C3, C4

Wake up Events

- Power Button
- USB Keyboard/Mouse/Devices
- Ring In
- PME#
- RTC Alarm
- MAC
- Audio

SIS648MX/963 System Architecture



M661MX/648MX/M652 Feature Comparison



	<i>M661MX</i>	<i>648MX</i>	<i>M652</i>
South Bridge	963	963	962
FSB	533/400	533/400	533/400
DRAM	DDR400	DDR400	DDR333
AGP	8X/3.5	8X/3.5	4X/3.0
Gfx	Real256E	No	Real256
DirectX	DX9 SW compliant	NA	DX7

PS: M661MX/648MX are Pin Compatible

SiS Technology Advantage

- ❖ SiS HyperStreaming Technology
- ❖ SiS Ultra-AGP II TM Advantage

SiS HyperStreaming Technology

- ❖ HyperStreaming Architecture
- ❖ Performance Advantages

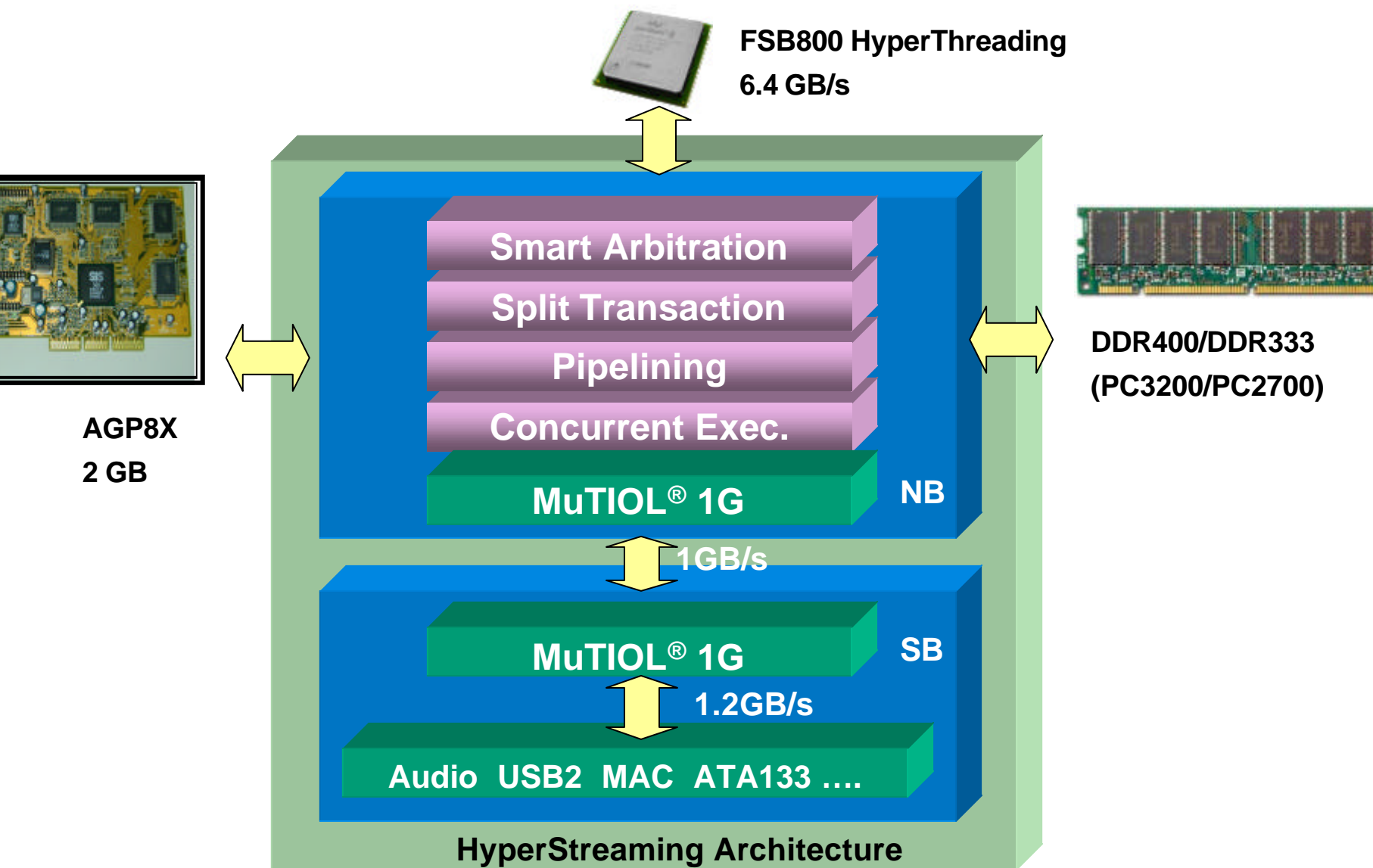


■ **“HyperStreaming”** Makes Streams of Data Flow All Over the Paths with More

- ✓ Efficiently
- ✓ Concurrently
- ✓ Smoothly
- ✓ Intelligently

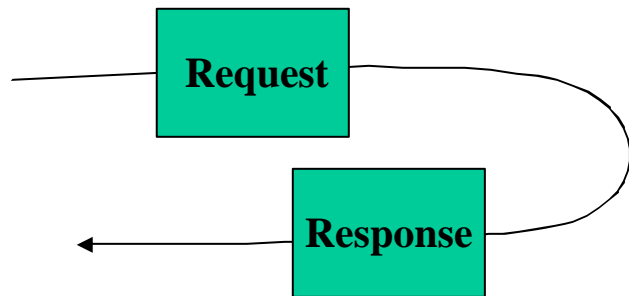
■ **Optimizing System for**

- **“Low Latency”** with Single Stream
- **“Pipelining”** and **“Concurrent Execution”** with Multiple Stream
- **“Prioritized Channel”** with Specific Stream
- **“Smart Flow Control”** and **“Intelligent Arbitration”** with Smart Stream

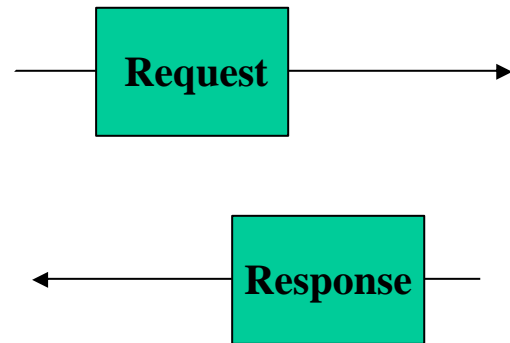
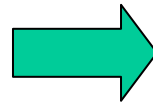


HyperStreaming Links Fast Together

Split Transaction:

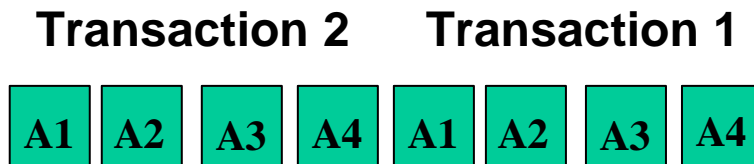
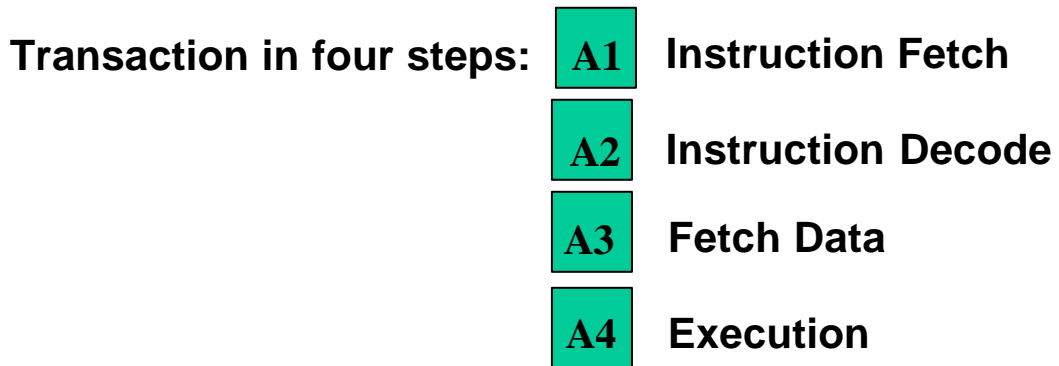


Bus occupied until “Response” is returned. Bus can not be released until the request and response phase completed.

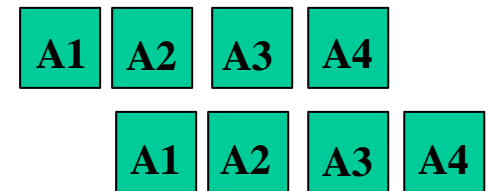
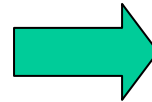


Bus released after “Request” phase and Bus can be used by next transaction (either request or response), then be occupied while the response is return. The Bus utilization is better.

Pipelining Transaction:

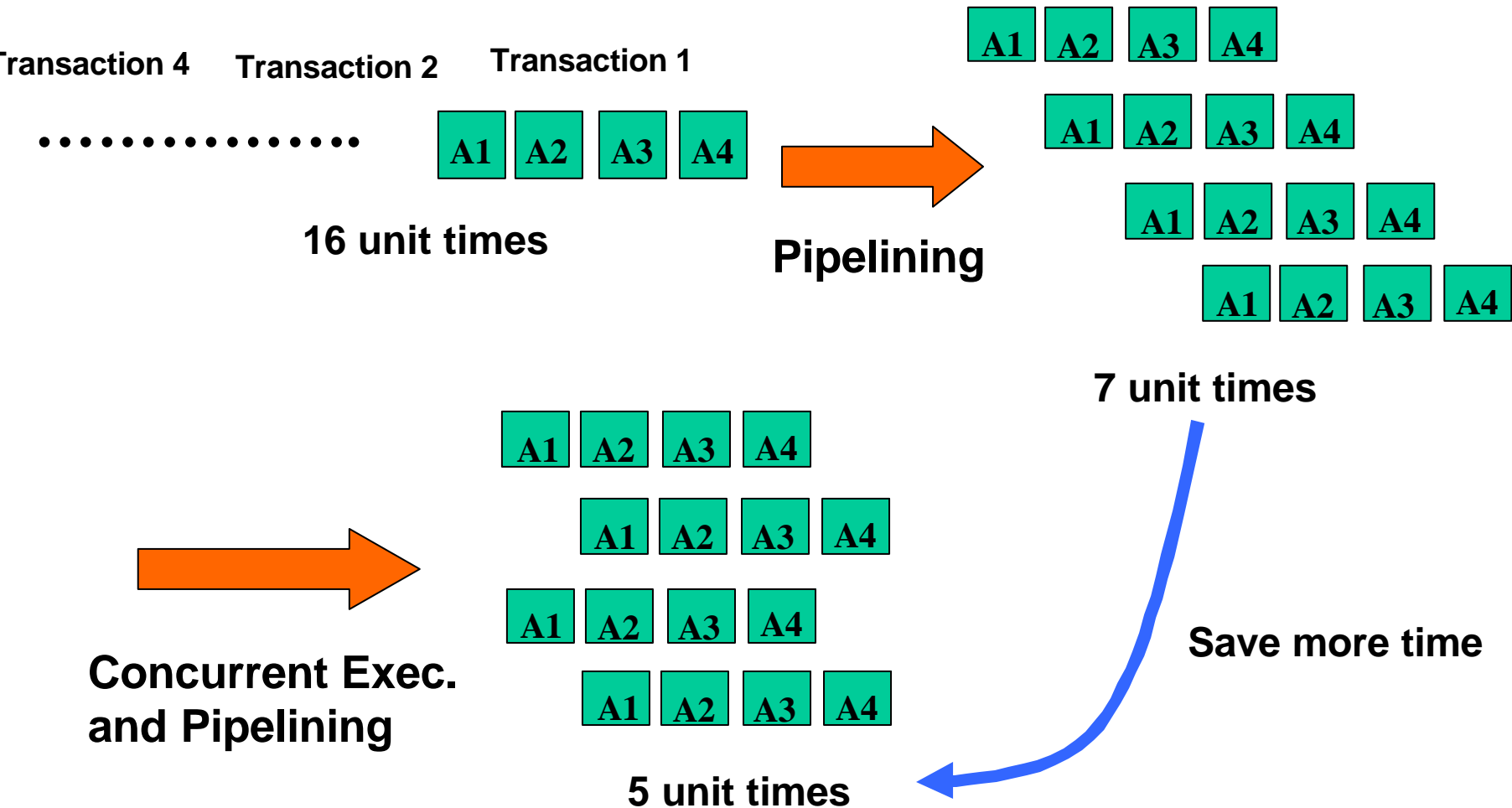


8 unit times



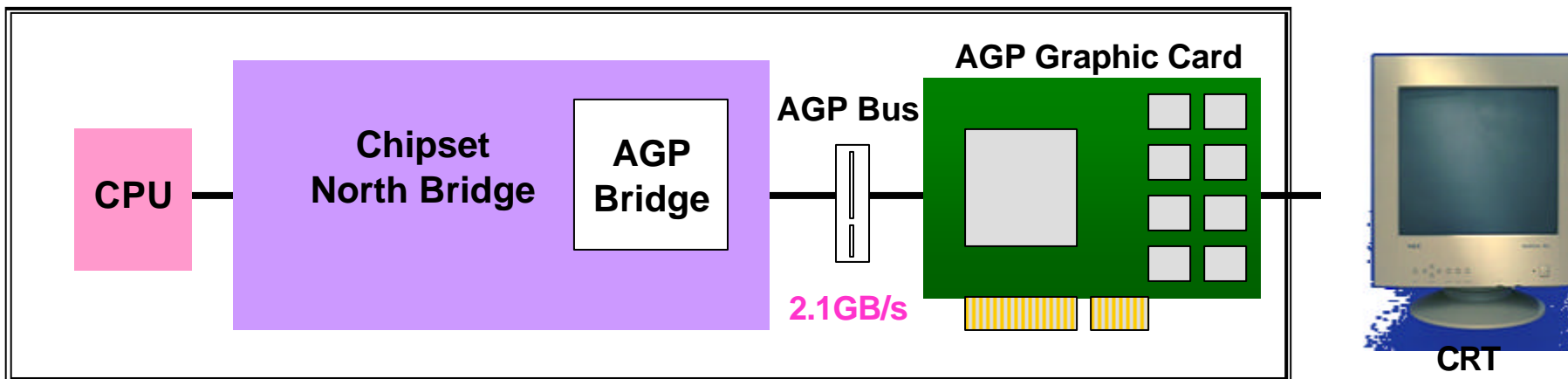
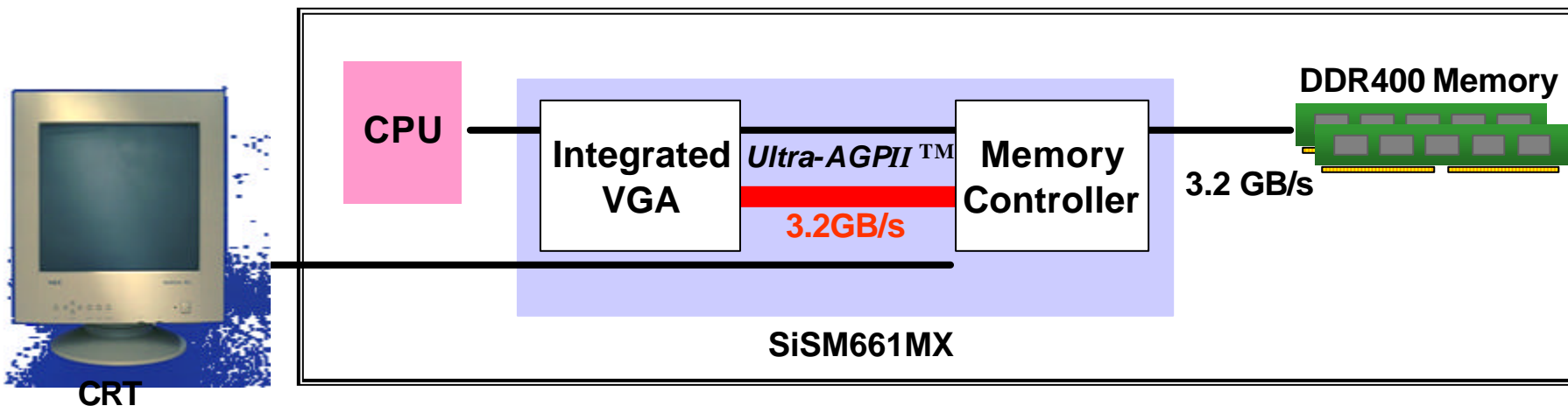
5 unit times

Concurrent Exec. and Pipelining Transaction:



SiS Ultra-AGP II TM Advantage

- ❖ High Bandwidth @ 3.2GB/s > AGP 8X @ 2.1 GB/s
- ❖ Shorter Data Transfer Path vs. External AGP Path
- ❖ Bus Cycle Advance Pipeline vs. Pipeline



Software Information

❖ **SiS Unified VGA Driver**

- Backward compatible w/M650/651/650/740 family
- Support Win98SE, WinME, Win2000 and WinXP

❖ **SiS Unified AGP Driver**

- Backward compatible w/648/650/645/735/635/730/630 family

❖ **SiS7012 Unified Audio Driver**

- Backward compatible w/962/961/735/635 Family

❖ **SiS Unified LAN Driver**

- Backward compatible w/962/961/735/635/730/630 family

❖ **SiS Unified IDE Driver for ATA133**

- Backward compatible w/962/961 family

❖ **USB2.0**

- WinXP SP1 and later one in-box USB2 driver support SiS USB2
- Win2000 and WinXP USB2 logo driver v1.00 released
- Win98SE and WinME USB2 driver supported from the third party.

North Bridge- M661MX:

Sample : **NOW**

Mass Production : **NOW**

North Bridge- 648MX:

Sample : **NOW**

Mass Production : **NOW**

North Bridge- M652:

Sample : **NOW**

Mass Production : **NOW**

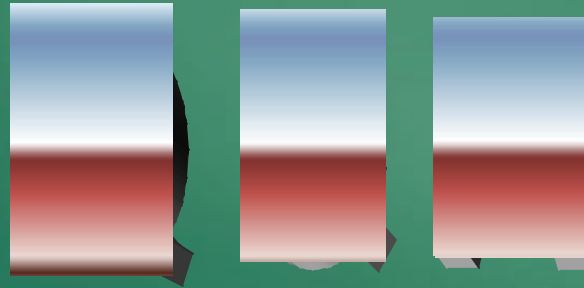
South Bridge- 963:

Sample : **NOW**

Mass Production : **NOW**

Third Party Information





❖ Thank You !!

